FAIRCHILD SEMICONDUCTOR™

February 1994
Revised June 2001

# 74LCX16244
# Low Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

## General Description

The LCX16244 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The LCX16244 is designed for low voltage (3.3V) $V_{CC}$ applications with capability of interfacing to a 5V signal environment.

The LCX16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

## Features

- 5V tolerant inputs and outputs
- 4.5 ns $t_{PD}$ max, 10 µA $I_{CCQ}$ max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V $V_{CC}$ supply operation
- ±24 mA output drive
- Uses patented noise/EMI reduction circuitry
- Functionally compatible with 74 series 16244
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

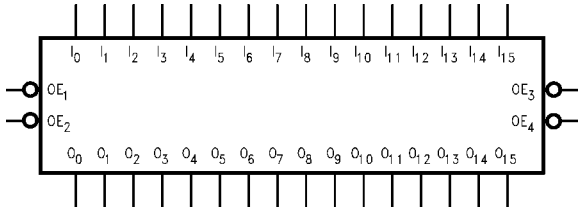
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74LCX16244GX (Note 1) | BGA54A | 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL] |
| 74LCX16244MEA (Note 2) | MS48A | 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide |
| 74LCX16244MTD (Note 2) | MTD48 | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

**Note 1:** BGA package available in Tape and Reel only.

**Note 2:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

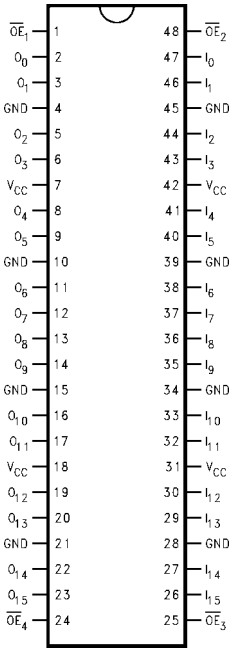
## Logic Symbol



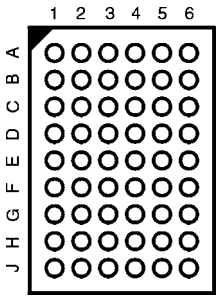

 

## Connection Diagrams

**Pin Assignment for SSOP and TSSOP**




**Pin Assignment for FBGA**




**(Top Thru View)**

## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OE}_n$ | Output Enable Input (Active LOW) |
| $I_0$–$I_{15}$ | Inputs |
| $O_0$–$O_{15}$ | Outputs |
| NC | No Connect |

## FBGA Pin Assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | $O_0$ | NC | $\overline{OE}_1$ | $\overline{OE}_2$ | NC | $I_0$ |
| **B** | $O_2$ | $O_1$ | NC | NC | $I_1$ | $I_2$ |
| **C** | $O_4$ | $O_3$ | $V_{CC}$ | $V_{CC}$ | $I_3$ | $I_4$ |
| **D** | $O_6$ | $O_5$ | GND | GND | $I_5$ | $I_6$ |
| **E** | $O_8$ | $O_7$ | GND | GND | $I_7$ | $I_8$ |
| **F** | $O_{10}$ | $O_9$ | GND | GND | $I_9$ | $I_{10}$ |
| **G** | $O_{12}$ | $O_{11}$ | $V_{CC}$ | $V_{CC}$ | $I_{11}$ | $I_{12}$ |
| **H** | $O_{14}$ | $O_{13}$ | NC | NC | $I_{13}$ | $I_{14}$ |
| **J** | $O_{15}$ | NC | $\overline{OE}_4$ | $\overline{OE}_3$ | NC | $I_{15}$ |

## Truth Tables

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_1$ | $I_0$–$I_3$ | $O_0$–$O_3$ |
| L | L | L |
| L | H | H |
| H | X | Z |

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_2$ | $I_4$–$I_7$ | $O_4$–$O_7$ |
| L | L | L |
| L | H | H |
| H | X | Z |

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_3$ | $I_8$–$I_{11}$ | $O_8$–$O_{11}$ |
| L | L | L |
| L | H | H |
| H | X | Z |

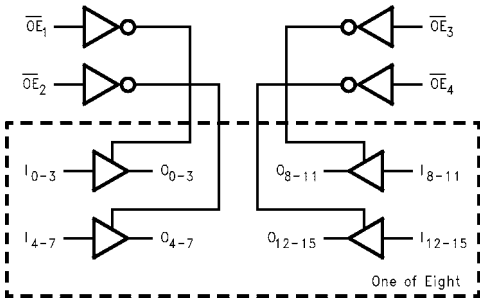
| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_4$ | $I_{12}$–$I_{15}$ | $O_{12}$–$O_{15}$ |
| L | L | L |
| L | H | H |
| H | X | Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

## Functional Description

The LCX16244 contains sixteen non-inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

## Logic Diagram



## Absolute Maximum Ratings(Note 3)

| Symbol | Parameter | Value | Conditions | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 to +7.0 | | V |
| $V_I$ | DC Input Voltage | −0.5 to +7.0 | | V |
| $V_O$ | DC Output Voltage | −0.5 to +7.0 | Output in 3-STATE | V |
| | | −0.5 to $V_{CC}$ + 0.5 | Output in HIGH or LOW State (Note 4) | V |
| $I_{IK}$ | DC Input Diode Current | −50 | $V_I$ < GND | mA |
| $I_{OK}$ | DC Output Diode Current | −50<br>+50 | $V_O$ < GND<br>$V_O$ > $V_{CC}$ | mA |
| $I_O$ | DC Output Source/Sink Current | ±50 | | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | ±100 | | mA |
| $I_{GND}$ | DC Ground Current per Ground Pin | ±100 | | mA |
| $T_{STG}$ | Storage Temperature | −65 to +150 | | °C |

**Note 3:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 4:** $I_O$ Absolute Maximum Rating must be observed.

## Recommended Operating Conditions (Note 5)

| Symbol | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Operating | 2.0 | 3.6 | V |
| | | Data Retention | 1.5 | 3.6 | |
| $V_I$ | Input Voltage | | 0 | 5.5 | V |
| $V_O$ | Output Voltage | HIGH or LOW State | 0 | $V_{CC}$ | V |
| | | 3-STATE | 0 | 5.5 | |
| $I_{OH}/I_{OL}$ | Output Current | $V_{CC}$ = 3.0V–3.6V | | ±24 | mA |
| | | $V_{CC}$ = 2.7V | | ±12 | |
| $T_A$ | Free-Air Operating Temperature | | −40 | 85 | °C |
| $\Delta t/\Delta V$ | Input Edge Rate, $V_{IN}$ = 0.8V–2.0V, $V_{CC}$ = 3.0V | | 0 | 10 | ns/V |

**Note 5:** Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = −40°C to +85°C | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | | 2.7–3.6 | 2.0 | | V |
| $V_{IL}$ | LOW Level Input Voltage | | 2.7–3.6 | | 0.8 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $I_{OH}$ = −100 µA | 2.7–3.6 | $V_{CC}$ − 0.2 | | V |
| | | $I_{OH}$ = −12 mA | 2.7 | 2.2 | | V |
| | | $I_{OH}$ = −18 mA | 3.0 | 2.4 | | V |
| | | $I_{OH}$ = −24 mA | 3.0 | 2.2 | | V |
| $V_{OL}$ | LOW Level Output Voltage | $I_{OL}$ = 100 µA | 2.7–3.6 | | 0.2 | V |
| | | $I_{OL}$ = 12 mA | 2.7 | | 0.4 | V |
| | | $I_{OL}$ = 16 mA | 3.0 | | 0.4 | V |
| | | $I_{OL}$ = 24 mA | 3.0 | | 0.55 | V |
| $I_I$ | Input Leakage Current | 0 ≤ $V_I$ ≤ 5.5V | 2.7–3.6 | | ±5.0 | µA |
| $I_{OZ}$ | 3-STATE Output Leakage | 0 ≤ $V_O$ ≤ 5.5V<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | 2.7–3.6 | | ±5.0 | µA |
| $I_{OFF}$ | Power-Off Leakage Current | $V_I$ or $V_O$ = 5.5V | 0 | | 10 | µA |
| $I_{CC}$ | Quiescent Supply Current | $V_I$ = $V_{CC}$ or GND | 2.7–3.6 | | 20 | µA |
| | | 3.6V ≤ $V_I$, $V_O$ ≤ 5.5V | 2.7–3.6 | | ±20 | µA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH}$ = $V_{CC}$ −0.6V | 2.7–3.6 | | 500 | µA |

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $C_L = 50pF$, $R_L = 500\ \Omega$ | | | | Units |
|---|---|---|---|---|---|---|
| | | $V_{CC} = 3.3V \pm 0.3V$ | | $V_{CC} = 2.7V$ | | |
| | | Min | Max | Min | Max | |
| $t_{PHL}$ | Propagation Delay | 1.5 | 4.5 | 1.5 | 5.2 | ns |
| $t_{PLH}$ | Data to Output | 1.5 | 4.5 | 1.5 | 5.2 | |
| $t_{PZL}$ | Output Enable Time | 1.5 | 5.5 | 1.5 | 6.3 | ns |
| $t_{PZH}$ | | 1.5 | 5.5 | 1.5 | 6.3 | |
| $t_{PLZ}$ | Output Disable Time | 1.5 | 5.4 | 1.5 | 5.7 | ns |
| $t_{PHZ}$ | | 1.5 | 5.4 | 1.5 | 5.7 | |
| $t_{OSHL}$ | Output to Output Skew (Note 6) | | 1.0 | | | ns |
| $t_{OSLH}$ | | | 1.0 | | | |

**Note 6:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$). Parameter guaranteed by design.

## Dynamic Switching Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = 25°C$ Typical | Units |
|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | 0.8 | V |
| $V_{OLV}$ | Quiet Output Dynamic Valley $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | –0.8 | V |

## Capacitance

| Symbol | Parameter | Conditions | Typical | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = Open, $V_I = 0V$ or $V_{CC}$ | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$, f = 10 MHz | 20 | pF |

## AC LOADING and WAVEFORMS Generic for LCX Family

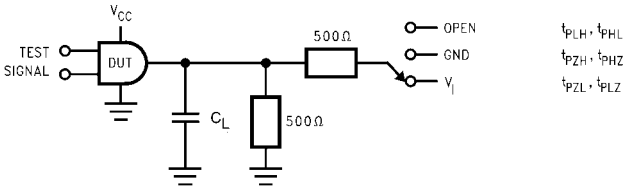
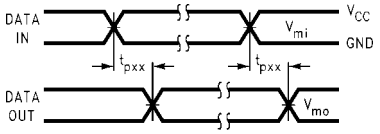
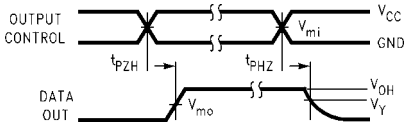



**FIGURE 1. AC Test Circuit ($C_L$ includes probe and jig capacitance)**

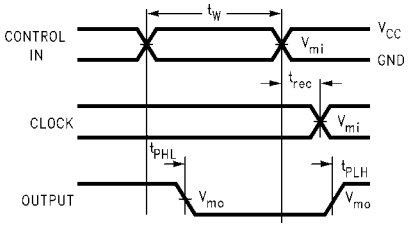
| Test | Switch |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6V at $V_{CC}$ = 3.3 ± 0.3V<br>$V_{CC}$ x 2 at $V_{CC}$ = 2.5 ± 0.2V |
| $t_{PZH}$,$t_{PHZ}$ | GND |



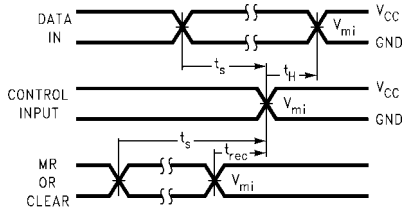

**Waveform for Inverting and Non-Inverting Functions**



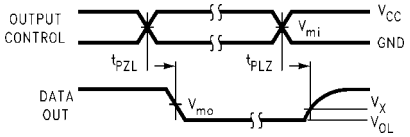

**3-STATE Output High Enable and Disable Times for Logic**



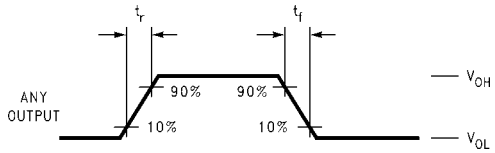

**Propagation Delay. Pulse Width and $t_{rec}$ Waveforms**




**Setup Time, Hold Time and Recovery Time for Logic**




**3-STATE Output Low Enable and Disable Times for Logic**

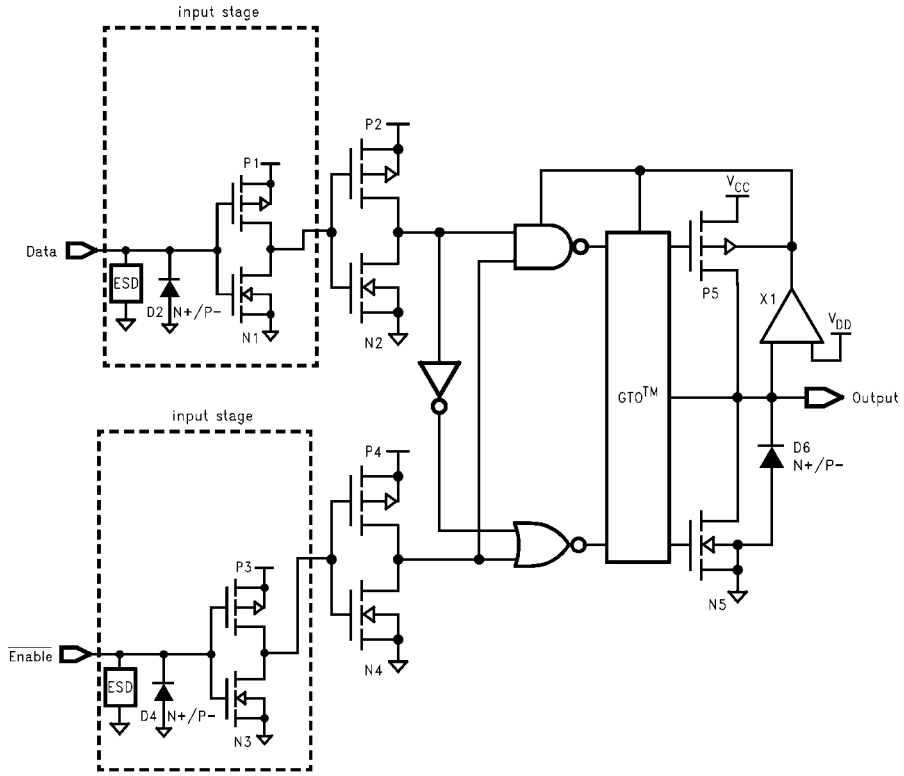



**$t_{rise}$ and $t_{fall}$**

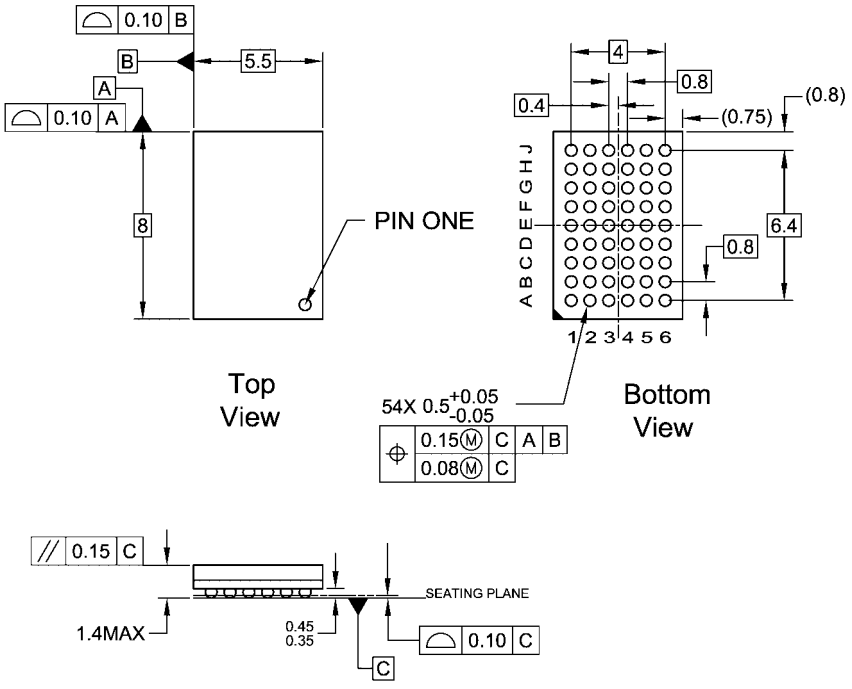
**FIGURE 2. Waveforms**
**(Input Characteristics; f =1MHz, $t_R$ = $t_F$ = 3ns)**

| Symbol | $V_{CC}$ | | |
|---|---|---|---|
| | **3.3V ± 0.3V** | **2.7V** | **2.5V ± 0.2V** |
| $V_{mi}$ | 1.5V | 1.5V | $V_{CC}$/2 |
| $V_{mo}$ | 1.5V | 1.5V | $V_{CC}$/2 |
| $V_x$ | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.15V |
| $V_y$ | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.15V |

## Schematic Diagram Generic for LCX Family



## Physical Dimensions inches (millimeters) unless otherwise noted



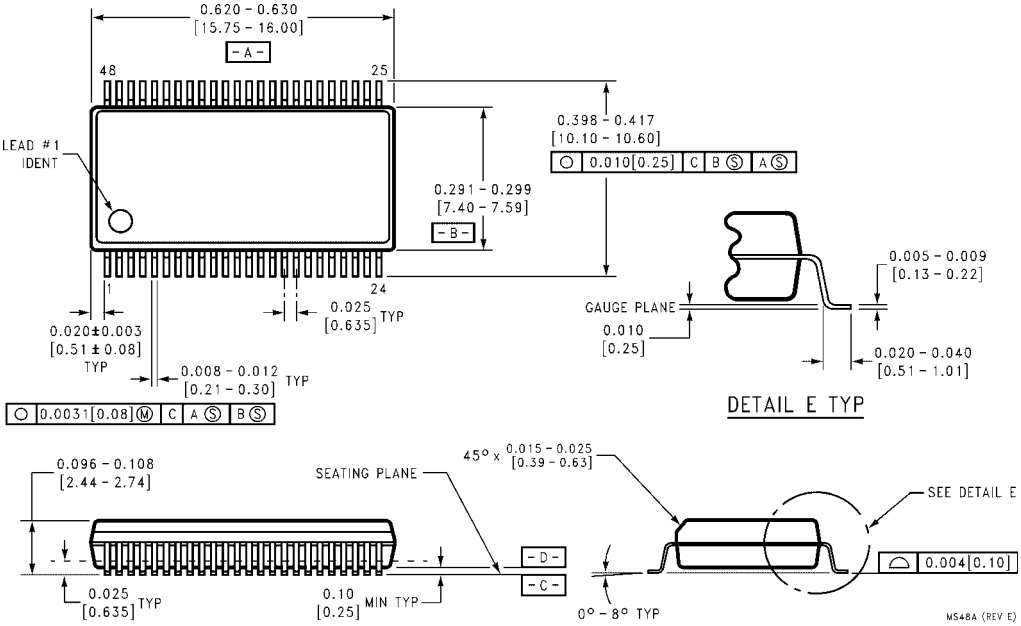

NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

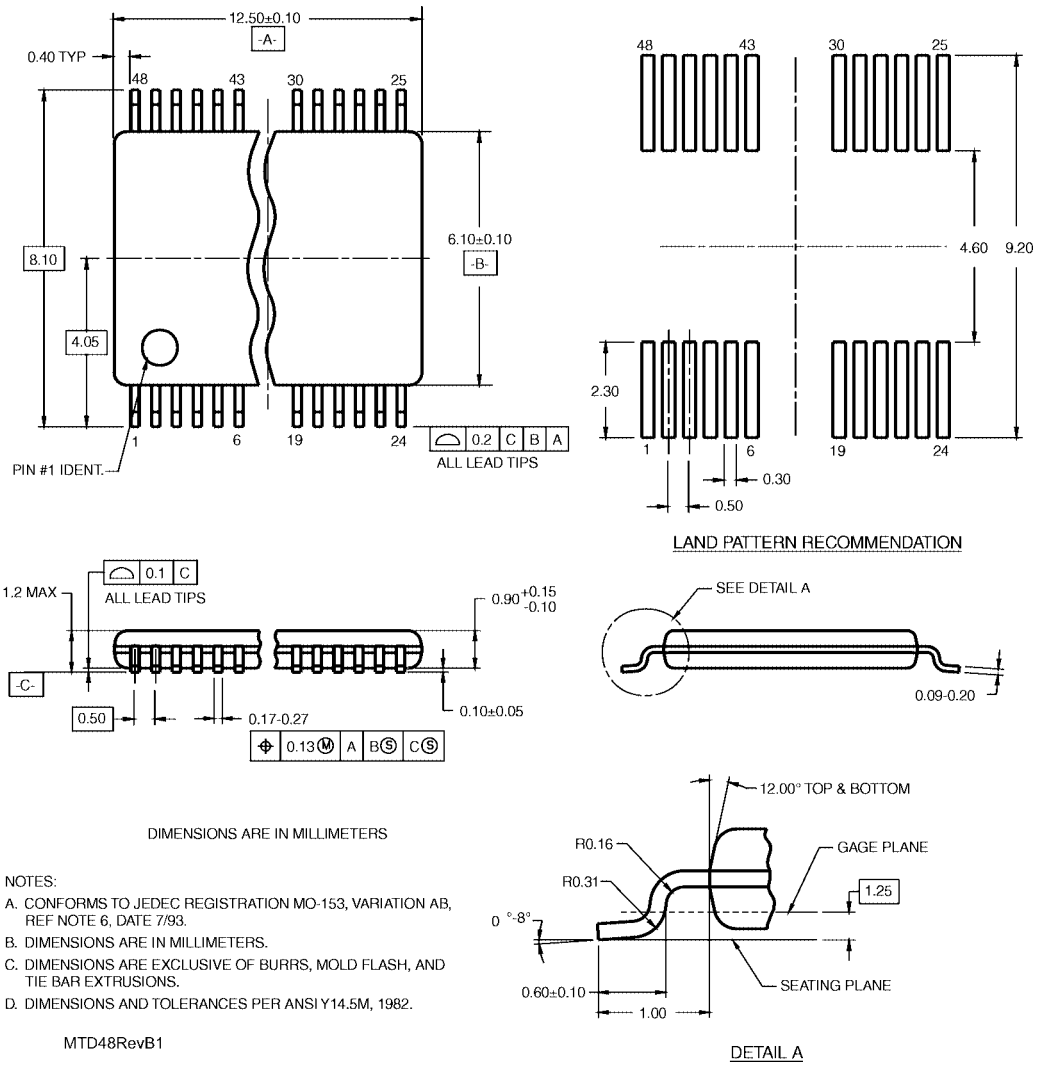
**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide**
**Package Number BGA54A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide**
**Package Number MS48A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD48**



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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